



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/811,892

03/30/2004

Eun-sup Kim

1793.1184

1320

21171

7590

01/22/2008

STAAS & HALSEY LLP

SUITE 700

1201 NEW YORK AVENUE, N.W.

WASHINGTON, DC 20005

EXAMINER

SITTA, GRANT

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

01/22/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/811,892	Applicant(s) KIM, EUN-SUP	
	Examiner Grant D. Sitta	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 September 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>8/05/2005 and 3/30/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 6, 13, 19, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (Korean publication No. 2001-55653), hereinafter Kim.

3. In regards to claim 6, Kim teaches controlling (fig. 1 (110)) an inverter (fig. 1 (90)) to drive the backlights (fig. 1 (80)) in synchronization with a first horizontal synchronization ((fig. 2 (a) "the timing controller (40) is generated the fluorescent lamp control signal having the off period synchronized to the vertical synchronizing signal (a)") signal in a digital video signal when video signals are input; determining whether a display mode has been changed (fig. 2 (a)); inputting an inverter, if the display mode is changed (fig. 2 (a)), to control the inverter to not drive the backlights(seventh paragraph from the end Under the "Structure and Function of the Invention"); checking whether the display mode change is completed (tenth paragraph from the end Under the "Structure and Function of the Invention"); and inputting an inverter on signal to the inverter if the display mode change ("The horizontal synchronizing signal (b) corresponding to the whole row line for..." fifth paragraph from the end Under the

"Structure and Function of the Invention") is completed so as to control the inverter to drive the backlights in synchronization with a second horizontal synchronization signal.

4. In regards to claims 13 and 21, Kim teaches driving the backlights (fig. 1 (80)) in synchronization with a first synchronization ((fig. 2 (a) "the timing controller (40) is generated the fluorescent lamp control signal having the off period synchronized to the vertical synchronizing signal (a)") signal driven according to various inputs in a video determining (vertical synchronization) whether a display mode has been changed (fig. 2 (a)) stopping (fig. 2 (c)) the driving if the display mode is changed (fig. 2 (a and c)); checking whether the display mode change is completed; and resuming driving the backlights in synchronization with a second synchronization (fig. 2 (b)) signal in a video signal if the display mode change is completed (Under the "Structure and Function of the Invention").

5. In regards to claims 19 and 20, Kim teaches a panel (fig. 1 "panel" (50)) and an inverter (fig. 1 (90) "inverter circuit") in a liquid crystal display having backlights (fig. 1 (80)), which are synchronized ("the fluorescent lamp control signal (C) is synchronized to the vertical synchronizing signal") with one another to avoid oscillatory interference there between and to remove noise from a screen, wherein the inverter is turned off (seventh paragraph from the end Under the "Structure and Function of the Invention") during a display mode change to prevent the backlights from being turned off (seventh paragraph from the end Under the "Structure and Function of the Invention").

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claim 1,3,7,8,10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al (7,098,903) hereinafter, Park in view of Hong-Gyun Kim (Korean publication No. 2001-55653), hereinafter Kim.

3. In regards to claims 1, Park discloses the limitations of a liquid crystal display (fig. 1), having a liquid crystal panel (fig. 1 ((230) "flat panel display panel")) and backlights (col. 5, lines 65-70)), comprising:

a signal converter (Fig. 1 (310)) to convert selectively input analogue video signals into digital video (Fig. 1 (ADC)) signals in synchronization with a first

predetermined sampling clock signal (col. 5, lines 30-36));

a scaler (fig. 1 (340) lines 27-32) to sample the digital video signals at a preset resolution in synchronization with a second predetermined sampling clock signal, and to extract a horizontal synchronization signal from the sampled digital video signals (col. 5, lines 30-36)); Examiner notes a horizontal synchronization signal is carried on the input signal and must be extracted to display formats, such as VGA., and is an inherent element in displays.

a panel driver (fig. 1 (220)) to display the digital video signals on the liquid crystal panel (fig. 1 ((230) "flat panel display panel"));

a controller (fig. 1 (340) lines 27-32) to detect the extracted horizontal synchronization signal from the digital video signals to determine a display mode (col. 5, lines 30-36)), to output the first and second predetermined sampling clock signals to the signal converter and the scaler (fig. 1 (340) lines 27-32), respectively, according to the determined display mode, and to generate inverter on/off signals (Fig. 3 signal to (110)) whenever the display mode is changed (col. 2, lines 5-10) and (col. 5 25-45). Examiner notes while the reference does not explicitly say the horizontal synchronization signal is used to drive the scaler and signal converter, one skilled in the art will recognize a clock is needed for both these devices and the will be set to the horizontal synchronization signal and an inverter (fig. 3 (110)),

Park differs from the claimed invention in that Park does not disclose inverter to drive the backlights in synchronization with the detected horizontal synchronization signal and the inverter on/off signals.

However, Kim teaches a system and method for inverter to drive the backlights (fig. 1 (80)) in synchronization (fig.2 (a and b)) with the detected horizontal synchronization signal (fig. 2 (b)) and the inverter on/off signals (fig.2 c) ("Under the "Structure and Function of the Invention").

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Park to include the use of a means to control the backlight as taught by Kim in order to prevent ghost as stated in (Under, "Technical Problems to be solved by the Invention.").

4. In regards to claim 3, Kim teaches the controller generates and outputs the inverter off signals to the inverter when the display mode is changed, and continues generating and outputting the inverter off signals until the horizontal synchronization signal is detected (5th paragraph from bottom under, "Technical Problems to be solved by the Invention." "The horizontal synchronization signal (b) corresponding to the whole row line for one vertical synchronization signal (a) of a number is applied").

5. In regards to claim 7, Kim teaches checking if the display mode change is not completed. (fig 2 (a-c))

6. In regards to claim 8, Kim teaches further comprising initially skipping the determining the inputting the inverter off signal, and the checking operations if the user has not changed the display mode (fig. 2 (a-c))

7. In regards to claim 10, Park teaches wherein the determining comprises determining whether the display mode is changed from a PC (analog) to that of a DTV (DVI-D) (fig. 3 Analog RGB and DVI-D input).

8. In regards to claim 14, Park teaches repeating the checking if the display mode change is not complete (fig. 3). Park discloses a display device with multiple inputs having all the features claimed except for the specific checking if the display mode is not changed. Although it the "checking" is not explicitly stated it would have been obvious to one skilled in the art since a clock is an inherent part of a display device and would be necessary to determine when an input device is connected to the display device.

9. Claim 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et. al (US 6,404,145) hereinafter, Saito in view of Park.

10. In regards to claim 4, Saito teaches a system and method where a display mode changes while video signals (fig. 3 video signal) are displayed and applying backlight off signals (fig. 3 Backlight control voltage (OFF)) to the inverter while the display mode is

changing (fig. 3 Video Signal changing from displaying to off), and applying backlight on signals (fig. 3 Backlight control voltage) to the inverter (taught by Park) when a horizontal synchronization signal is detected (col. 5, lines 38-45),

Saito differs from the claimed invention in that Saito does not explicitly disclose an inverter.

However, Park teaches an inverter (fig. 3 (110)).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Saito to include the use of an inverter as taught by Park in order to drive the backlight (col. 4, lines 32-35).

11. In regards to claim 5, Saito teaches wherein the horizontal synchronization signal begins to cause a transient effect when the display mode is changed (fig. 2 (12)) Examiner notes that (12) inherent nature of the transistor will cause a transient effect from the power source (8).

12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Kim, and further in view of Yoo et. al (US 2003/0214478) hereinafter, Yoo.

13. In regards to claim 2, Park and Kim discloses the limitations of claim 1,

Park and Kim differs from the claimed invention in that Park and Kim does not disclose how the means by which the inverter controls the backlight.

However, Yoo teaches a system and method for a pulse width modulator (fig. 9 (140)) to generate pulse width modulation signals [0122], which are synchronized with the horizontal synchronization signal (Kim figs. 1 and 2), and to turn the pulse width modulation signals on or off ([0122] "on/off") according to the inverter on/off signals generated by the controller [0122] "The PWM control part is turned on or off by an external on/off control signal"; a switching transformer (fig. 9 (150) which controls the switch Q1) to switch a power supply on or off (fig. 9 Vin (DC)) according to the pulse width modulation signals (fig. 9 signal from 140); and a lamp (fig. 9 (110) [0112] "lamp array") which radiates light using the power supplied by the switching transformer ([0111-0126]

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Park and Kim to include the use of PWM as taught by Yoo in order to control the inverter and backlight assembly as stated in (fig. 9 the lamp driving device, [0112-0126]).

14. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Kim, in view of Ogoro et al (6,891,525) hereinafter, Ogoro.

15. In regards to claim 11, Park discloses the limitations of claim 6

Park differs from the claimed invention in that Park does not disclose wherein the checking last until the second horizontal synchronization signal is generated

However, Ogoro teaches a system and method for wherein the checking last until the second horizontal synchronization signal is generated " (Fig. 7 col. 7-8, lines 60-35 of Ogoro).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Park to include the use of checking until the second signal is generated as taught by Ogoro in order for "detecting a currently set operation mode..." as stated in (Fig. 7 col. 2, lines 20-30 of Ogoro).

16. In regards to claim 12, Ogoro teaches where the checking comprises determining whether the second horizontal synchronization signal exist in the video signals. (Fig. 7 col. 7-8, lines 60-35 of Ogoro).

17. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Kim, in view of Anderson et. al (US 6,678,005) hereinafter, Anderson.

18. In regards to claim 9, Park discloses the limitations of claim 1

Park differs from the claimed invention in that Park does not disclose

However, Anderson teaches a system and method for recognizing key signals (Examiner notes key signals will be necessary when the user is prompted with the choice) as display mode change signals if the video signals are those of a PC (Abstract "PC") and are displayed (fig. 3, (370)) when the user inputs the key signals to change the video signals (fig. 3 (360)). (col. 2, lines 20-50 of Anderson).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Park to include the use of means recognizing key signals as display mode change when the video signal are those of a PC as taught by Anderson in order to "...accommodate for concurrent presence of multiple video signals in a PC or TV environment." as stated in (col. 2, lines 15-20 of Anderson).

19. Claims 15, 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Kim, in view of Ogoro.

20. In regards to claim 15, Park discloses the limitations of claim 13

Park differs from the claimed invention in that Park does not explicitly disclose skipping the determining, the inputting, the stopping, and the checking operations if the display mode is not changed.

However, Ogoro teaches a system and method for "mode setting selecting" (Fig. 7 col. 7-8, lines 60-35 of Ogoro).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Park to include the use of "mode setting selecting" as taught by Ogoro in order to provide for mode selection and lowering power consumption as stated in (col. 2, lines 15-65 of Ogoro).

21. In regards to claim 16, Ogoro teaches determining comprises recognizing key signals as display mode change signals. (col. 3-4, lines 70-5 Ogoro).

22. In regards to claim 17, Ogoro teaches checking last until the second synchronization signal is generated (Fig. 7 col. 7-8, lines 60-35).

23. In regards to claim 18, Ogoro teaches where the checking comprises determining whether the synchronization signal exist in the video signal ((Fig. 7 col. 7-8, lines 60-35 of Ogoro).

24. Claims 22,23,24,25 and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loveridge et al (US 6,545,688) hereinafter Loveridge, in view of Cui et. al (US PUB 7,119,786) hereinafter, Cui.

25. In regards to claim 22, Loveridge discloses the limitations of a signal converter to convert a video signal into a digital video signal in synchronization with a first sampling clock signal (fig. 3, col. 8, lines 30-40);

a scaler to sample the digital video signal in synchronization with a second sampling clock signal (fig. 3 (370)), and to extract a first synchronization signal therefrom (fig. 3, col. 8, lines 19-30, "HSYNC");

a panel driver to display (fig. 1b (160)) the digital video signals on the liquid crystal panel (fig. 1b (170)); a controller to detect the synchronization signal (col. 8, lines

19-30, "HSYNC") from the digital video signal to determine a display mode (Examiner notes "display mode" is very broad and can encompass such thing as a change in scale.), to output the first and second sampling clock signals ("The specific sampling time points may be controlled by a source clock..." since there are multiple points there must be more than one clock) to the signal converter and the scaler (col. 8, lines 5-50), respectively, according to the determined display mode, and to generate inverter on/off signals whenever the display mode is changed;

Loveridge differs from the claimed invention in that Loveridge does not disclose an inverter to drive the backlights in synchronization with a second synchronization signal and the inverter on/off signals.

However, Cui teaches a system and method for an inverter to drive a backlight in synchronization with a second synchronization signal and the inverter on/off signal (Fig. 5 col. 5, lines lines 35-70 of Cui).

It would have been obvious to one of ordinary skill in the art, at the time of the invention; to modify Loveridge to include the use of an inverter with the backlight in synchronization with a second signal and on/off signal as taught by Cui in order to maintain a display image quality regardless of variances in backlight brightness of a flat-panel display..." as stated in (col. 2, lines 55-60 of Cui).

26. In regards to claim 23, Loveridge teaches wherein the controller determines a display mode (fig. 3 (360), col. 9, lines 30-37, Loveridge).

27. In regards to claim 24, Loverridge teaches wherein a controller outputs the first and second sampling clock signals to the signal convert (Fig. 3 (380) and (390)) and the scaler (Fig. 3 370) respectfully according to the determined display mode (Fig. 3 col. 9, lines 28-36, Loverridge).

28. In regards to claim 25, Cui teaches wherein the inverter comprises a pulse width modulator to generate pulse width modulations signals synchronized with the first synchronization signal to turn the pulse width modulation signals on and off according to the inverter on/off signals generated by the modulator. (Fig. 5, col. 35-70, Cui "Power Sequencer" is a PWM (See Patent 6,766,222 Fig. 2)).

29. In regards to claim 26, Cui teaches wherein the inverter further comprises a switching transformer to switch a power supple on or off according to the pulse width modulation signals input from the pulse width modulator. (Fig. 5, col. 35-70, Cui "Power Sequencer" is a PWM Inherent in a "Power Sequencer" (See Patent 6,766,222 Fig. 3)).

30. In regards to claim 27, Cui teaches wherein the inverter further comprises a lamp to radiate light using the power supplied by the switching transformer. (Fig. 5, col. 35-70, Cui). Examiner notes the Applicant is merely claiming an inverter built into the backlight and would have been obvious to one skilled in the art.

31. In regards to claim 28, Cui teaches wherein a controller generates and outputs inverter off signals to the inverter when the display mode is changed, and continues generating and outputting inverter off signals until the second synchronization signal is detected. (Fig. 5 "D" remote on signal and remote off signal).

32. In regards to claim 29, see claim 22 and an inverter which is synchronized with the liquid crystal panel to avoid oscillatory interference therebetween, to drive the backlight in synchronization signal with a second synchronization signal and the inverter on/off signals (fig. 5 col. 5, lines 35-70, "D" remote on and off).

Response to Arguments

1. Applicant's arguments with respect to claims 1, 13, 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

Application/Control Number:
10/811,892
Art Unit: 2629

Page 16

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta
December 6, 2007


AMARE MENGISTU
SUPERVISORY PATENT EXAMINER